

**IN THE SPECIFICATION:**

Please replace paragraph [0037] with the following:

A novel aspect of the invention is the use of the cesium ion implant 100 post silicide electrical test in order to tune the threshold voltage,  $V_t$ . As such, the invention centers both the nFET and pFET threshold voltages,  $V_t$ , which are slightly too positive (for the desired application) at the PSP electrical test. In particular, those processes which are responsible for determining the  $V_t$  (at the point that silicide processing is completed) are engineered to result in a nominal  $V_t$  for both nFET and pFET configurations, which is more positive than the final desired  $V_{ts}$  ( $V_{tf}$ ) when the BEOL processing is complete. For example, if the tolerance of the  $V_t$  is given by  $dV_t$ , then the process is designed (e.g. by choice of halo ion-implant doses and energies) to yield a threshold voltage of  $V_{ts} + dV_t$ . When a given wafer is fabricated and tested at PSP, a particular value of  $V_t$  is measured and will have some particular offset,  $V_{toff}$ , above the final target  $V_{tf}$ . A cesium ion dose normal to the channel surface is then calculated for each type of FET, using  $N_{Cs} = 2C_{ox} \times V_{toff}/Qe$ , where  $C_{ox}$  is the capacitance per unit area of the gate electrode to the channel, and  $Qe$  is the unit electronic charge (approximately  $1.6 \times 10^{-19}$  C). The dose of ions actually ion-implanted must be adjusted to account for the geometry of the structure. For instance, when ion-implantation is normal to the wafer surface and the FinFET presents a channel which is normal to the wafer, then the implanted dose must be a factor of the fin height divided by the gate oxide thickness times the calculated normal dose.

Please replace the abstract with the following:

~~A method and structure for tuning a threshold voltage of nFET and pFET devices in a double-gate CMOS integrated circuit structure, wherein the method comprises performing a PSP (post silicide processing) electrical test on the double-gate CMOS integrated circuit structure, determining nFET and pFET threshold voltages during the PSP test, and implanting the double-gate CMOS integrated circuit structure with an alkali metal ion, wherein the step of implanting adjusts the nFET and pFET threshold voltages by an amount required to match desired off-currents for the nFET and pFET devices. According to the method, prior to the step of performing, the method comprises forming a fin structure over an isolation layer, forming source/drain regions over the fin structure, depositing a gate oxide layer adjacent to the source/drain regions, and forming a gate region over the gate oxide layer and the fin structure. The metal ion comprises any of cesium and rubidium.~~

A field effect transistor (FET) comprising an isolation layer, a source region positioned over the isolation layer, a drain region positioned over the isolation layer, a bifurcated silicide gate region positioned over the channel region, and a gate oxide layer adjacent to the gate region, wherein the gate oxide layer comprises an alkali metal ion implanted at a dosage calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said FET, wherein the alkali metal ion comprises any of cesium and rubidium.